

Time: 3hrs

[Total Marks:80]

- N.B. :** (1) Question No 1 is Compulsory.
 (2) Attempt any three questions out of the remaining five.
 (3) All questions carry equal marks.
 (4) Assume suitable data, if required and state it clearly.

- 1 Attempt any FOUR [20]
 a State Working of TG logic with proper diagram
 b Explain Flash memory in brief.
 c For n-channel MOSFET $V_T = 1.75 \text{ V}$, $V_{GS} = 5 \text{ V}$, $V_{DS} = 2 \text{ V}$, $I_D = 120 \text{ A}$, $COX = 51.72 \text{ nF/CM}^2$, $\mu_n = 400 \text{ CM}^2/\text{S}$. Find the region of operation and W/L ratio.
 d Explain MOSFET electrical characteristics.
 e Write short note on clock distribution.
- 2 a Explain P-MOS fabrication with neat and clean diagram. [10]
 b Consider a CMOS inverter with following parameters: [10]
 nMOS $V_{TN} = 0.6 \text{ V}$ $K_n = 200 \mu\text{A/V}^2$
 pMOS $V_{Tp} = -0.7 \text{ V}$ $K_p = 80 \mu\text{A/V}^2$ $K_r = 2.5$
 Calculate noise margin. The power supply voltage is $V_{DD} = 3.3 \text{ V}$.
- 3 a Design SR Latch using CMOS logic and draw its layout [10]
 b i) Explain short channel effects in VLSI [10]
 ii) Implement carry circuit of 4 bit carry lookahead adder.
- 4 a Realize the expression for AND gate using the following logic style. [10]
 1. Clocked CMOS logic
 2. Pseudo NMOS
 3. Dynamic PMOS
 4. Domino Logic
 b Draw and explain 6-T SRAM with neat and clean diagram. Explain read and write condition with equations. [10]
- 5 a Implement using CMOS logic 1) 1-Bit full adder 2) DFF using TG. [10]
 b State and explain different types of ROM memory. Draw 4 *4 bit NAND based array to store the following data in respective memory locations. [10]

Memory address	Data
1000	1101
0100	1001
0010	1010
0001	1001

- 6 a Illustrate RTL design of 3 TAP Serial FIR filter with HLSM,FSM and datapath. Calculate hardware required for 100 TAP filter. [10]
 b Draw and explain VTC characteristics of CMOS inverter in detail. [10]